Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for reducing voiding between a first layer and a second layer formed over said first layer during a semiconductor annealing process, the method comprising:
forming a counter tensile layer over said second layer, wherein said counter tensile layer is selected from a material such that an opposing directional stress is created between said counter tensile layer and said second layer, with respect to a directional stress created between said first layer and said second layer.

[c2] The method of claim 1, wherein said counter tensile layer is selected to be the same material as said first layer.

[c3] The method of claim 2, wherein said first layer and said counter tensile layer comprise a refractory metal.

[c4] The method of claim 3, wherein said refractory metal comprises cobalt.

[c5] The method of claim 4, wherein said second layer comprises a titanium nitride cap layer.

[c6] A method for forming a metal silicide contact for a semiconductor device, the method comprising:
forming a refractory metal layer over a substrate, including active and non-active area of said substrate;
forming a cap layer over said refractory metal layer; and
forming a counter tensile layer over said cap layer,
wherein said counter tensile layer is selected from a material such that an opposing directional stress is created between said counter tensile layer and said cap layer, with respect to a directional stress created between said refractory metal layer and said cap layer.

[c7] The method of claim 6, wherein said counter tensile layer is selected to be the same material as said refractory layer.

[c8] The method of claim 7, wherein said refractory metal layer and said counter tensile layer comprise cobalt.

[c9] The method of claim 8, wherein said cap layer comprises a titanium nitride cap layer.

[c10] The method of claim 6, wherein:
said refractory metal layer is formed at a thickness of about 4 to about 7 nanometers;
said cap layer is formed at a thickness of about 10 to about 20 nanometers; and

said counter tensile layer is formed at a thickness of about 10 to about 30 nanometers.

[c11] The method of claim 6, wherein:
said refractory metal layer is formed at a thickness of about 4 to about 7 nanometers;
said cap layer and said counter tensile layer are formed at a combined thickness of about 15 to about 30 nanometers.

[c12] The method of claim 6, further comprising annealing the substrate so as to cause portions of said refractory metal layer to react with active areas of said substrate.